Remarks

Reconsideration of the application and allowance of all pending claims are respectfully requested. Claims 1-18 remain pending.

In the Office Action, dated December 3, 2004, claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. (U.S. Patent No. 5,784,393). Applicant respectfully, but most strenuously, traverses this rejection for the reasons herein. **Applicant respectfully requests that careful consideration be given to the remarks, including those directed to the dependent claims.**

In one aspect, applicant's invention is directed to error detection and correction of system-wide errors on interconnecting address, data and control lines. Single or multiple bit errors in various components of a data processing system, including those arising in interfaces, such as non-integrated intermittent interconnections, are able to be detected and corrected. To accomplish this, parity bits are generated in one portion of the data processing system, such as the sending portion, and the parity bits are tested in a second portion, such as the receiving portion, to detect one or more errors. The one or more errors are then corrected in the second portion. This allows intermittent errors occurring with, for instance, solder connections, mating connector pins or other types of mechanical connections to be detected and corrected.

In one particular aspect, applicant claims a method of providing error detection and correction in an interface between two portions of a data processing system. The method includes, for instance, generating, in a first portion of the data processing system, parity bits corresponding to a plurality of bits of the interface; transmitting across the interface the parity bits together with the plurality of bits of the interface; testing, in a second portion of the data processing system, that the parity bits correspond to the plurality of bits for which parity was encoded; and detecting and correcting, in the second portion of the data processing system, one or more errors in the plurality of bits for which parity was encoded. Thus, in this aspect of applicant's claimed invention, applicant detects and then corrects errors in a second portion of the data processing system, which is different than the portion that generated the parity bits. This is distinct from the teachings of Byers et al.

Assuming *arguendo* that Byers teaches error correction, Byers does not teach that the error correction is performed in a different portion of the data processing system than the portion that generated the parity bits, as claimed by applicant. Instead, Byers explicitly teaches that error correction is performed in the same portion as the generating, i.e., the transmitting portion. Byers goes to great lengths to describe how all of the error detection should be performed by only the transmitter user. For example, Byers states:

> A transmitting user may provide a data word and a number of corresponding parity bits to the bus via the output buffer. However, unlike the prior art fault detection schemes, the receiving user may not be capable of regenerating the parity bits and performing the compare function as described above. In the exemplary embodiment, the data word and the number of parity bits may be provided back into the transmitting user, via the input buffers of the transmitting user, wherein a parity check may be performed by the transmitting user. (Col. 4, lines 13-23)

Thus, if Byers was to describe error correction, it would teach that error correction would be performed in the same portion of the system, i.e., the transmitting portion, as the parity generation and error checking. One certainly would not be motivated by the teachings of Byers to have the parity generation separate from the error detection and correction, as claimed by applicant.

Further, it is stated in the Office Action that the error correction is the retransmitting of the data which is in error. Applicant respectfully submits that if retransmission is believed to be error correction, then the error correction is being performed by the transmitting portion, which is the same portion that is generating the parity bits. Thus, the error correction in Byers is not being performed by a second portion, as claimed by applicant. That is, the error correction is not being performed by a different portion than the parity generation. Therefore, applicant respectfully submits that independent claim 1, as well as independent claim 7, are patentable over Byers.

In addition to the above, applicant respectfully submits that the dependent claims are patentable for the same reasons as the independent claims, as well as for their own additional

features. The patentability of various of the dependent claims is described in further detail below.

As one example, dependent claim 13 explicitly recites that the parity generation is performed in the sending portion of the system and the error detection and correction are performed in the receiving portion. This is very different from the teachings of Byers. In Byers, if there is error correction, the error correction is performed in the sending portion. In particular, Byers teaches that data that is in error should be retransmitted by the sending portion. Since Byers teaches retransmission by the sending portion, Byers does not teach or suggest performing error detection and correction in the receiving portion, as claimed by applicant. Instead, Byers teaches the opposite of applicant's invention, assuming the error correction of Byers is retransmission.

Applicant respectfully submits that it is not indicated in the final Office Action where Byers teaches that the error correction is performed in the receiving portion of the data processing system, as claimed by applicant. Thus, for this reason, as well as for all of the above reasons, applicant respectfully submits that dependent claim 13 is patentable over Byers et al.

As a further example, dependent claims 3 and 9 indicate that the plurality of bits for which parity was encoded include data, address and control signals. Thus, in applicant's claimed invention, errors are detected and corrected for control signals, as well as for data and address lines. This is not taught or suggested in Byers. While Byers mentions control signals for various applications, Byers does not teach or suggest that errors arising from control signals are to be detected and corrected using parity bits. Byers is silent as to this feature.

Support for this rejection is indicated in FIG. 6, which has several components with the word "control" therein. However, applicant respectfully submits that neither FIG. 6 nor the description therein describes encoding parity for control signals. As a matter of fact, Byers explicitly teaches that parity is not encoded for control signals. For example, in FIG. 9A and the description associated therewith, parity bits are encoded for the data, as indicated at 904, but in the discussion of the control signals, no parity is encoded. So, although the

DSD bus of Byers has control signals, the parity and error correction of Byers does not apply to the control signals.

Further, in the description of the retransmission of the data, it is the data that is reviewed and a request is sent back to the source to retransmit the data. In the operation of Byers, there is no regeneration or recreating of control signals, only the data. Thus, applicant respectfully submits that Byers does not describe, teach or suggest in anyway, encoding parity for control signals nor of detecting and correcting errors in the control signals. Thus, applicant respectfully submits that Byers does not describe, teach or suggest this aspect of applicant's claimed invention.

As yet a further example, applicant recites that the detecting and correcting of errors are performed asynchronously (e.g., dependent claim 15). That is, the detection and correction of one or more errors are not reliant on clock cycles. This is contrary to Byers that specifically teaches that the detection of errors is reliant on multiple clock signals. The dependence upon a clock in Byers is explicitly shown by the many references in the text to bus cycles. Some of these references include the following:

> FIG. 9A – Bus cycles and bus clock (ref. #916);
>
> Timing diagrams in FIGs. 11, 12, 13:
>
> > 'BCLK AT NCR' – Bus clock is shown with diagram on first line at top of diagram;
>
> Col. 17, lines 1-3 – These lines describe an exemplary embodiment that initiates operation over multiple bus clock cycles;
>
> Col. 23, line 6 – '... bus clock...';
>
> Col. 23, line 11 – '...15 bus cycles.';
>
> Col. 25, lines 31, 62, '...bus clock cycle...' and references to timing diagrams;
>
> Col. 25 and Col. 26 – multiple references to timing diagrams and bus cycles;
>
> Col. 26, line 11'... 15 bus cycles.'

Thus, applicant respectfully submits that Byers does not describe, teach or suggest that the detecting and correcting of errors are performed asynchronously. Instead, Byers teaches just the opposite. Thus, applicant respectfully requests an indication of allowability for claim 15.

In another example, applicant recites in dependent claims 16 and 17 that the correcting comprises reconstructing one or more bits using the transmitted bits of the interface, and that the reconstruction is regardless of the nature of the error, respectively. First, Byers does not teach reconstructing one or more bits using the transmitted bits. If Byers teaches any correction at all, Byers teaches that the data in error is merely retransmitted. There is no reconstruction of the bits using the transmitted bits of the interface, as claimed by applicant. This is simply not taught in Byers.

Further, Byers does not teach reconstruction regardless of the nature of the error, as claimed by applicant. In Byers, data with errors is retransmitted only if it is a soft error. If it is a hard error, no retransmission is performed. Instead, an error is provided. Thus, Byers does not teach reconstructing of one or more bits using the transmitted bits of the interface, and further, it does not teach reconstruction regardless of the nature of the error. Thus, applicant respectfully requests an indication of allowability for dependent claims 16 and 17.

As a further example, applicant recites detecting and correcting multiple bit errors (e.g., dependent claim 18). Again, this is in contrast to Byers which only detects one error at a time. Further, if any correction is performed in Byers again, it is only of one error. There is no provision in Byers for detecting and correcting multiple bit errors. Even in the Office Action, it is stated "The Examiner would like to point out that Byers teaches (Col. 1, line 60-68) a single parity bit in conjunction with a multiple bit data word can detect a single bit error within the data word." It further goes on to state that methods have been developed for detecting multiple errors within multiple bit data words by providing multiple parity bits for each. However, applicant respectfully submits that they are claiming multiple bit error correction, as well as detection. There is no teaching in Byers of error correction of multiple bits.

Based on the foregoing, applicant respectfully requests that Byers does not describe, teach or suggest one or more aspects of applicant's invention. Further, applicant respectfully submits that if other art is being relied upon in any of the above rejections, that this art be cited, so that applicant has an opportunity to provide arguments with respect to the particular environment and features being claimed.

For all of the above reasons, applicant respectfully submits that all pending claims are patentable over Byers, and applicant respectfully requests an indication of allowability for such claims.

Should the Examiner wish to discuss this case with applicant's attorney, please contact applicant's attorney at the below listed number.

Respectfully submitted,

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